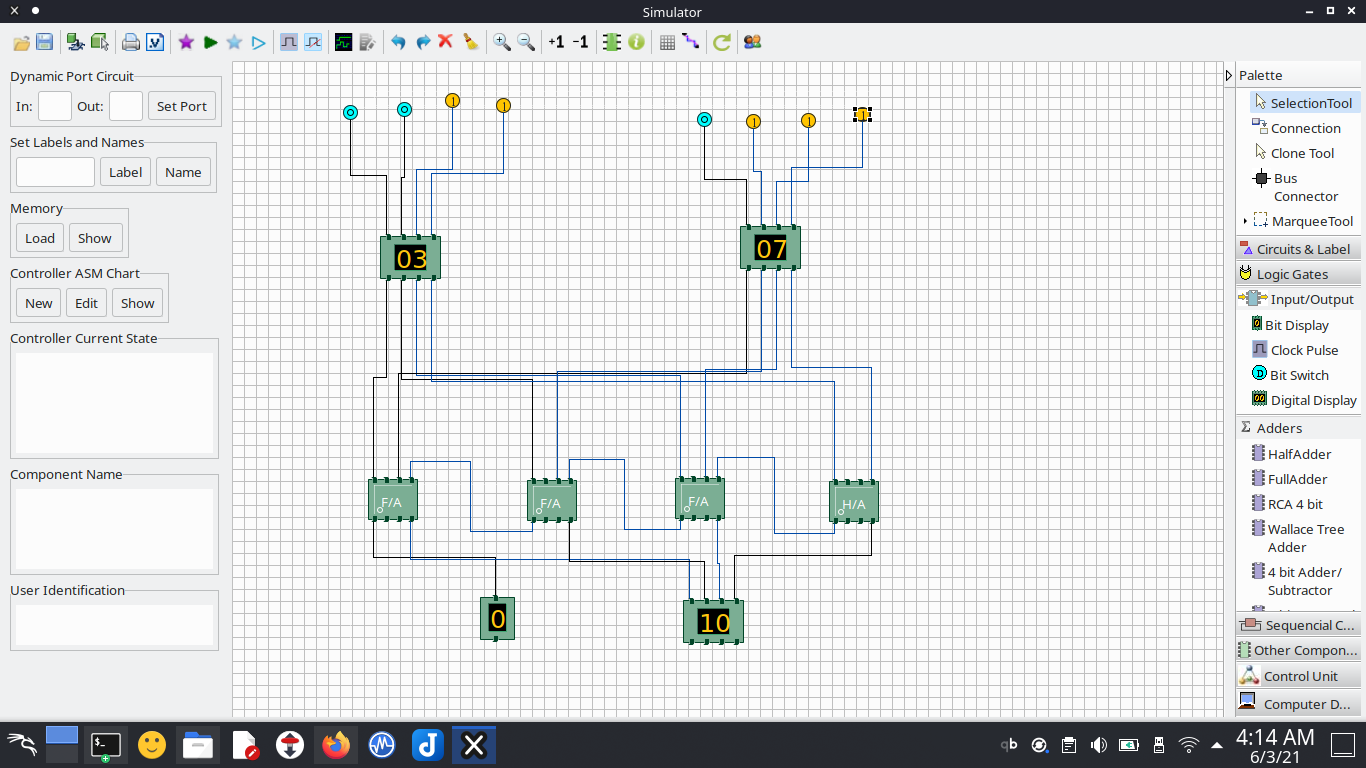
**Name – Ujjawal Mandhani**

**Batch – F6**

**Enroll no- 9918103237**

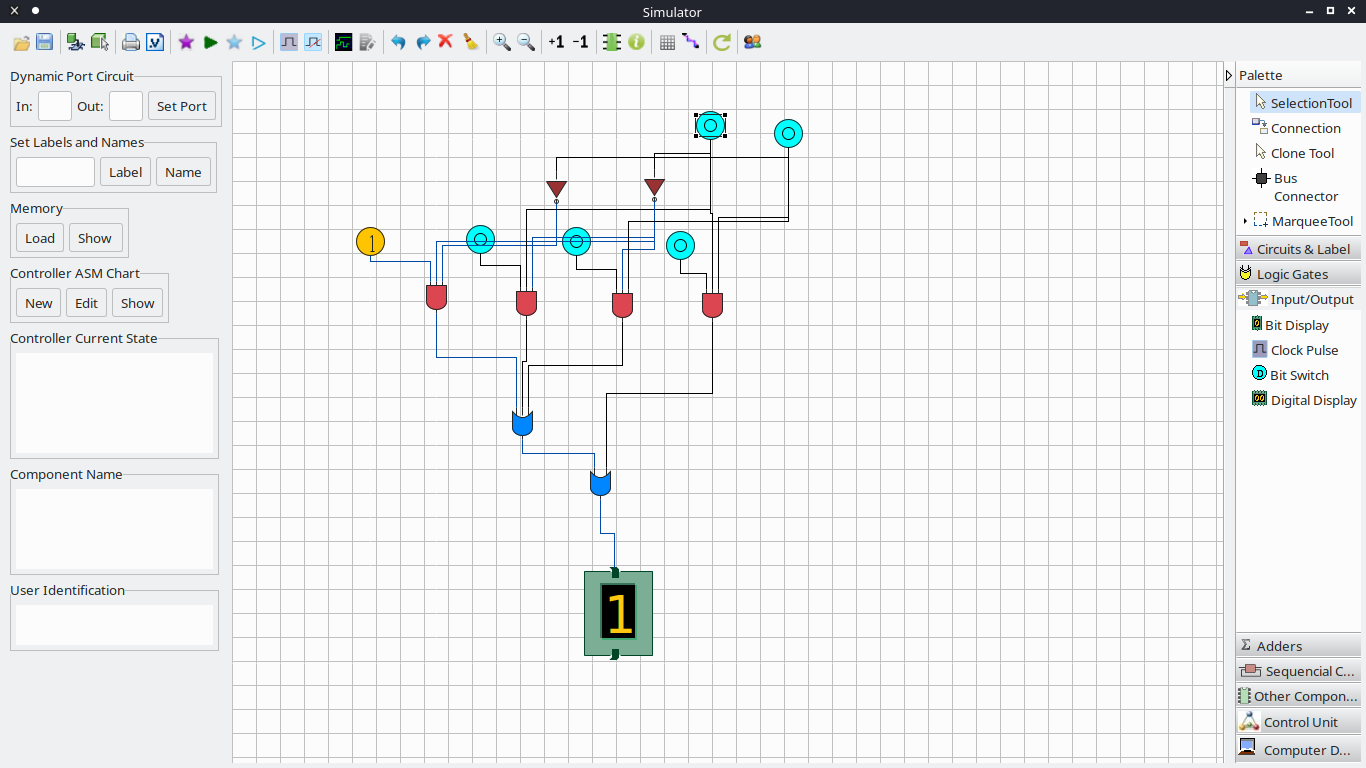
**COA – LAB 2**

**Question 1:** Reliazation of ripple adder logic gate

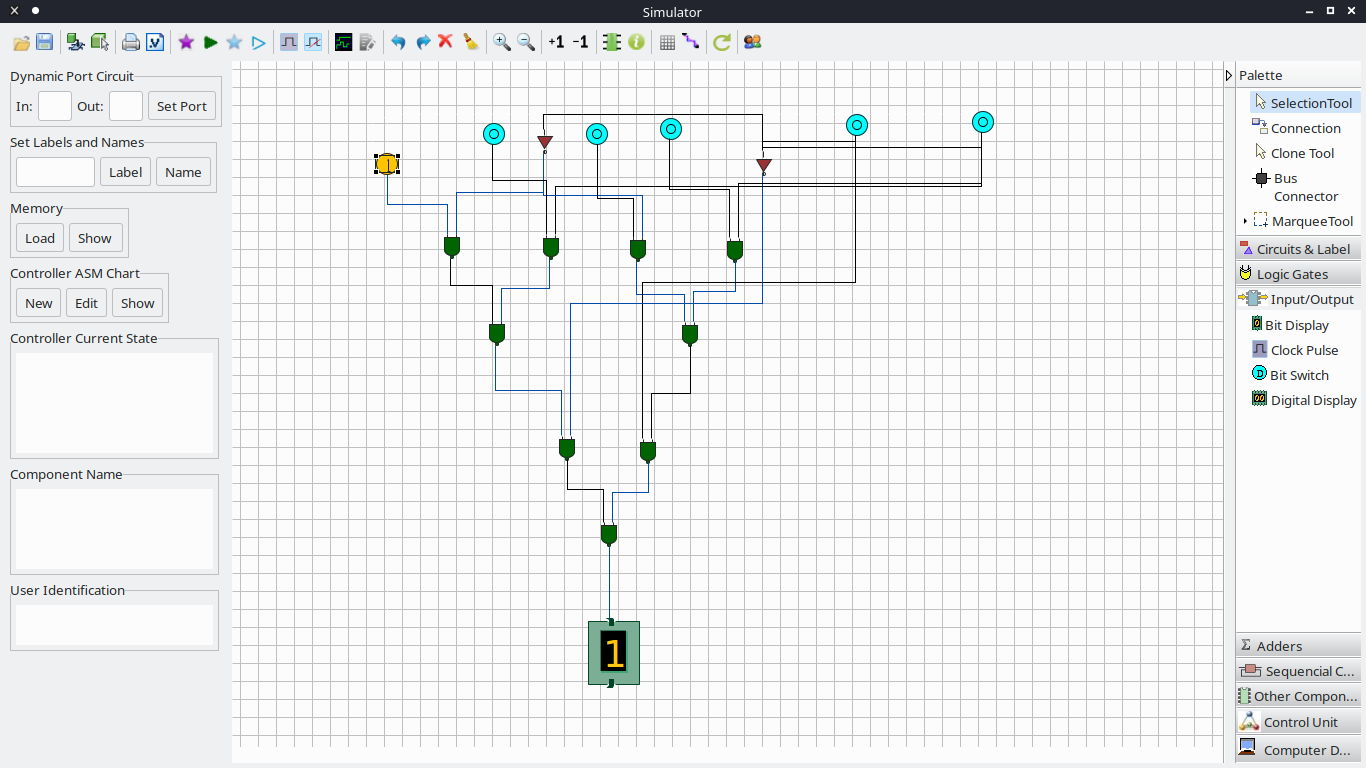


**Question 2:**Design the 4 x1 multiplexor circuit and realize the various input output logic based on

control.



**Question 3:** Design the 4X1 multiplexor with NAND gates logic circuits.

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